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Press Release

# EDAA Lifetime Achievement Award 2008 goes to Ernest S. KUH

***Grenoble, France, 2 February 2008 –*** The EDAA Lifetime Achievement Award 2008 goes to Ernest S. KUH.
The Lifetime Achievement Award is given to individuals who made outstanding contributions to the state of the art in electronic design, automation and testing of electronic systems in their life. In order to be eligible, candidates must have made innovative contributions which had an impact on the way electronic systems are being designed.

Past recipients have been Kurt ANTREICH (2003), Hugo DE MAN (2004), Jochen JESS (2005), Robert BRAYTON (2006) and Tom WILLIAMS (2007).

The Award will be presented at the plenary session of the 2008 DATE Conference, to be held 10-14 March in Munich, Germany.

Ernest S. KUH was born on October 2, 1928 in Beijing China. He attended Shanghai Jiao Tong University from 1945 to 1947; received the B.S. degree from the University of Michigan, Ann Arbor, in 1949; the S.M. degree from the Massachusetts Institute of Technology, Cambridge, in 1950; and the Ph.D. degree from Stanford University, Stanford California, in 1952. From 1952 to 1956 he was a member of the Technical Staff at Bell Telephone Laboratories in Murray Hill, New Jersey. He joined the EECS Department faculty at the University of California, Berkeley in 1956. From 1968 to 1972 he served as Chair of the Department; from 1973 to 1980 he served as Dean of the College of Engineering. He retired in 1993, and now holds the title of Professor in the Graduate School at Berkeley.

Prof. KUH's pioneering work has spanned a broad spectrum of topics in EDA physical design and circuit design, with concentration in the area of physical design and circuit simulation. He has made many pioneering and fundamental contributions in floorplanning, partitioning, placement, global routing, single row routing, channel routing, timing driven layout, and circuit simulation, and made great impact to the EDA research community and industry.

Prof. KUH's work on quadratic placement algorithm (as first presented in PROUD) led to the development of a whole new class of analytical placement techniques, which form the basis of commercial placement engines used by the EDA industry today.

The concept of the vertical constraint graph introduced in Prof. KUH's seminal work on graphe-theoretical approach to channel routing was fundamental to every channel router used in the research community and industry.

Prof. KUH's work on the BBL, and BEAR layout systems are the basis of many floorplanning systems in universities as well as industry.

Prof. KUH's pioneering work on the timing-driven placement and clock routing again opened the new era of timing-driven layout for deep submicron designs, and has inspired a new generation of EDA researchers and new startups in the past two decades.

Prof. KUH's work on StepWide Equivalent Conductance description of MOS transistors as implemented in the SWEC simulator has attracted many users in the IC industry.

Prof. KUH's work on techniques and algorithms for physical design has been pivotal in turning the design methodologies from manual "paper dolling" to automated layout. These techniques and algorithms have made it possible to layout large complex VLSI chips in the deep sub-micron regime and meet performance requirements while keeping the turnaround time manageable. These techniques are used widely by the EDA industry in commercial implementations of practical systems available to designers around the globe. They also form the foundation of follow-up research in many universities and the IC industry worldwide.

**More information and electronic version of this PR available at:**
**http://www.edaa.com/**
**B. COURTOIS, EDAA Chair, tel : +33 476 57 46 15, Bernard.Courtois@imag.fr**

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